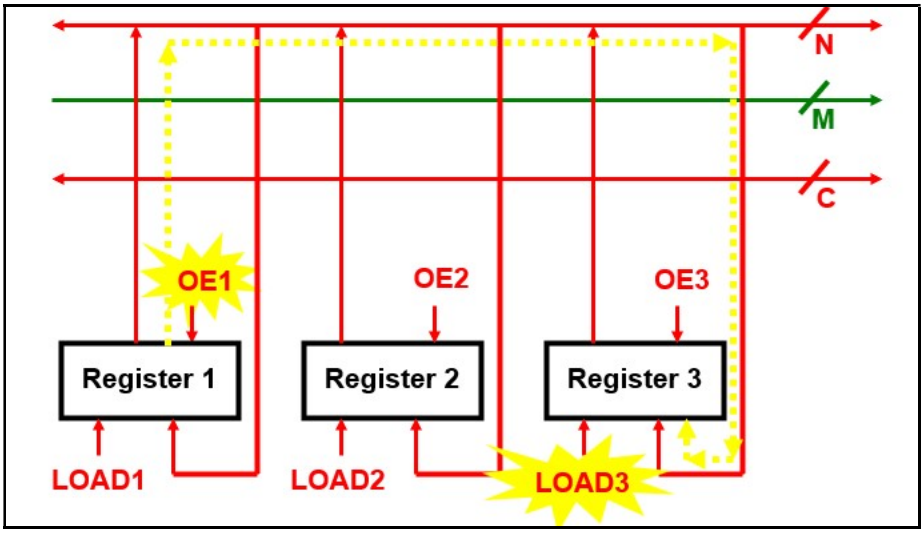
CANOS Project 1

Data Bus Design

(complete this project in groups of up to 3)

We start the CANOS course by looking at the high-level architecture of the MIPS CPU and some of its components. We discuss in lecture the fact that a digital signal containing multiple bits is called a bus, and that multiple registers can be connected to a single bus with the ability to both read from and write to it. In this way, the bus facilitates communication between registers and other components of the CPU.



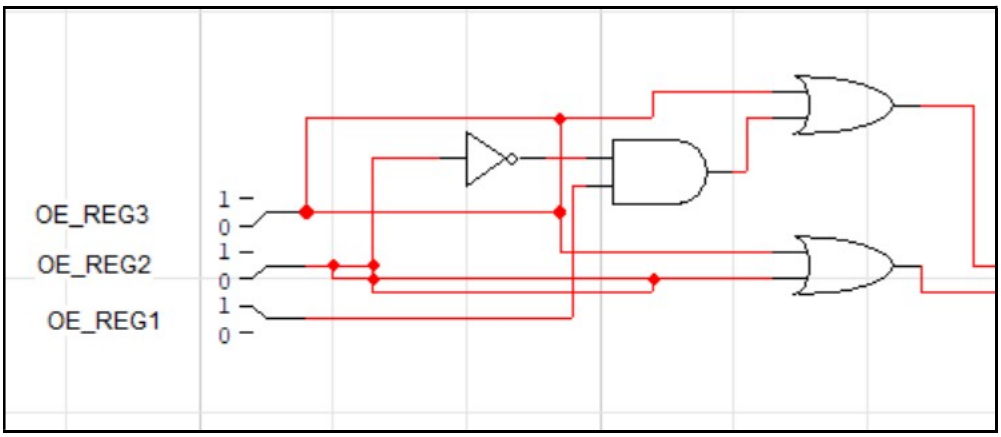
In this lab, you will design a two-way four-bit data bus that facilitates communication between three four-bit registers. The details of the design are up to you, but the finished design should be simulated in LogicWorks and have the following properties:

- The data bus consists only of a set of four wires.
- The three registers should be created using the 74_175 part.
- The design should be synchronous, with the registers loading on a clock pulse. Other components or the design may or may not be clocked; this is up to you.
- One register should take a user-defined 4 bit number as input. This can be done with the Hex Keyboard part
- The other two registers should load values directly from the bus. These registers should each have a “Load” flag that can be set high or low to determine whether that register will load from the bus on the next clock pulse. Both registers should be able to load from the bus at the same time.
- All three registers should have “Output Enable” flags that can be set high or low to determine whether each register will output its stored value to the bus. However, you must come up with

some way to prevent multiple registers from doing this at the same time and creating a logic value conflict on the bus.

Some Useful Tips

- The “Buffer-4 T.S.” part is a chip containing four tri-state buffers. This is very useful for enabling or disabling a register’s output to the bus.
- Below is the design for a simple priority encoder for a three-bit input. This may be useful for ensuring that only one output enable is active at once.



- Logic probes are useful for debugging your design. If a logic probe reads C, it means Conflict – that is, you are attempting to define 2 different logic levels at the same location in the circuit.
- Be sure to have a way to initialize your registers with a CLR signal.

Your submission should contain:

1.) (15 pts) Your working .cct LogicWorks circuit file. You are encouraged to document your circuit well and make it easy to understand. This means using a sensible component layout and labeling inputs and outputs clearly.

2.) (5 pts) A brief explanation of how the work was divided amongst your teammates.

3.) (5 pts) A paragraph or two of explanation about your design process. How did you set about designing this circuit? Did you try anything that ultimately did not work and had to be revised? What did you learn through completing this project?